IBM Monochrome Display and Parallel Printer Adapter

This adapter has dual functions. The first is to provide the interface to the IBM Monochrome Display. The second function is a parallel interface for the IBM 80 CPS Matrix Printer.

The monitor interface is designed around the Motorola 6845 CRT Controller module. There are 4K bytes of static memory on the card which are used for the display buffer. The memory is dual ported and may be accessed directly by the CPU. No parity is provided on the display buffer. A block diagram of the Monochrome Display function in on page 2-38.

The characteristics of the design are listed below:

- 80x25 Screen
- Direct Drive Output
- 9x14 Character Box
- 7x9 Character
- 18 Khz Monitor
- Character Attributes

The adapter supports 256 character codes. An 8K byte character generator contains the fonts for the character codes. The characters, values, keystrokes and screen characteristics are tabled in Appendix C. Of Characters, Keystrokes and Color.

Note: This Adapter when used with a display containing P39 Phospor, will not support a light pen!

Parallel Interface Description

This topic is discussed in full on pages 2-65 through page 2-69.



IBM Monochrome Display Adapter Block Diagram

Figure 14. IBM MONOCHROME DISPLAY ADAPTER BLOCK DIAGRAM

1.13 mm 1.0

System Channel Interface

Lines Used

This card uses the address and data bus, memory and I/O read/write signals, reset, I/O Ready, I/O Clock, and IRQ7.

Loads

Where possible, only one "LS" load is on the signals present at the I/O slot. Some of the address bus lines have two "LS" loads. No signal has more than two "LS" loads.

Special Timing

At least one wait state will be inserted on all memory and I/O accesses from the CPU. The duration of the wait-state will vary because the CPU/monitor access is synchronized with the character clock on this adapter.

To insure proper initialization of the attachment, the first instruction issued to the card must be to set the high resolution bit of the monitor output Port 1. (OUT PORT 3B8 = 01H). A CPU access to this adapter must never occur if the high resolution bit is not set.

System configurations which have two display adapter cards must insure that both adapters are properly initialized after a power on reset. Damage to either display may occur if not properly initialized.

Data Rates

For the IBM Monochrome Display Adapter, two bytes are fetched from the display buffer in 553 ns providing a data rate of 1.8M bytes/second.

Interrupt and DMA Response Requirements

- The display buffer can be written into, or read from using DMA.
- The parallel interface uses the +IRQ7 line. Interrupt becomes active when the acknowledge input is low, and interrupts are enabled via the control port.

Modes of Operation

The IBM Monochrome Display and Printer Adapter supports 256 character codes. In the character set are alphanumerics and block graphics. Each character in the display buffer has a corresponding character attribute. The character code must be an even address and the attribute code must be an odd address in the display buffer.



The adapter decodes the character attribute byte as defined above. The BLINK and INTENSITY bits may be combined with the FORE-GROUND and BACKGROUND bits to further enhance the character attribute functions listed below.

FUNCTION
NON DISPLAY UNDERLINE WHITE CHARACTER/ BLACK BACKGROUND

DMA Channels

The display buffer will support a DMA operation, however CPU wait-states will be inserted during DMA.

Interrupt Levels

Interrupt Level 7 is used on the parallel interface. Interrupts can be enabled or disabled via the Printer Control Port. The interrupt is a high level active signal.

I/O Address and Bit Map

The table below breaks down the functions of the I/O Address decode for the card. The I/O address decode is from '3B0' through '3BF'. The bit assignment for each I/O address follows:

I/O Address Function

3B0	Not Used
3B1	Not Used
3B2	Not Used
3B3	Not Used
3B4	6845 Index Register
3B5	6845 Data Register
3B6	Not Used
3B7	Not Used
3B8	CRT Control Port 1
3B9	Reserved
3BA	CRT Status Port
3BB	Reserved
3BC	Parallel Data Port
3BD	Printer Status Port
3BE	Printer Control Port
3BF	Not Used

The 6845 Index and Data Registers are used to program the CRT controller to interface to the high resolution Monochrome Display.

• CRT Output Port 1 (I/O Address '3B8')

Bit #	Function
0	+high resolution mode
1	Not used
2	Not used
3	+ video enable
4	Not used
5	+ enable blink
6,7	Not used
-	

- CRT Status Port (I/O Address '3BA')
 - Bit Function
 - 0 +Horizontal Drive
 - 1 Reserved
 - 2 Reserved

3

+B/W Video

IBM Monochrome Display

The high resolution IBM Monochrome Display unit attaches to the System Unit via two cables of approximately 3' (914 mm) in length. One cable is a signal cable which contains direct drive interface from the IBM Monochrome Display and Printer Adapter.

2 - 47

The second cable provides AC power to the display from the System Unit. This allows the System Unit power ON/OFF switch to also control the display unit. An additional benefit is a reduction in the requirements for wall outlets to power the system. The monitor contains an 12" (305 mm) diagonal 90° deflection CRT. The CRT and analog circuits are packaged in an enclosure so the display may either sit on top of the System Unit or on a nearby table top or desk. The unit has both brightness and contrast adjustment controls on the front available to the operator.

Operating Characteristics

Screen

High persistance green phosphor (P 39) with an etched surface to reduce glare. Unit displays an 80 character by 25 line screen with a 9 dot wide by 14 dot tall character box.

Video Signal

Maximum video bandwidth of 16.27 Mhz.

Vertical Drive

Screen refreshed at 50 Hz with 350 vertical lines of resolution and 720 lines of horizontal resolution.

Horizontal Drive

Positive level TTL compatible frequency, 18.432 Khz.

IBM Monochrome Direct Drive Interface and Pin Assignment





NOTE: Signal voltages are 0 - .6 Vdc at down level +5 Vdc at high level

HALDWALLS

Color/Graphics Monitor Adapter

The Color/Graphics Monitor Adapter is designed to attach a wide variety of TV frequency monitors and TV sets (user-supplied RF modulator required for TVs). It is capable of operating in black and white or color, and provides three video interfaces; a composite video port, a direct drive port, and connection interface for driving a user supplied RF modulator. In addition, a light pen interface is provided.

The adapter has two basic modes of operation; alphanumeric (A/N) and all points addressable graphics (APA). Additional modes are available within A/N and APA modes. In A/N mode, the display can be operated in a 40x25 mode for low resolution monitor and TVs or 80x25 mode for high resolution monitors. In both modes, characters are defined in an 8x8 box and are 5x7 with one line of descender for lowercase (both uppercase and lowercase characters are supported in all modes). In black and white mode, the character attributes of Reverse Video, Blinking and Highlighting are available. In color mode, there are 16 foreground colors and 8 background colors available per character. In addition, blinking on a per character basis is available.

The adapter card contains 16KB of storage; thus, for a 40x25 screen, 1000 bytes are used to store character information and 1000 bytes are used for attribute/color information. This means that up to 8 pages of screens can be stored in the adapter memory. Similarly, in an 80x25 mode, 4 pages of display screen may be stored in the adapter. The full 16KB storage on the display adapter is directly addressable by the processor allowing maximum software flexibility in managing the screen. In A/N color modes, it is also possible to select the screen border color. One of 16 colors may be selected.

In APA mode, there are two resolutions available; 320x200 and 640x200. In the 320x200, each (picture element) pel may have one of four colors. The background color (color 0) may be any of the 16 possible colors. The remaining 3 colors come from one of the two software selectable palettes. One palette contains red/green/brown, the other contains cyan/magenta/white.

The 640x200 mode is only available in black and white since the full 16KB of storage is used to define the on or off state of the pel.

The adapter operates in noninterlace mode at either 7 or 14 megahertz (Mhz) video bandwidth depending on the mode of operation selected.

In A/N mode, characters are formed from a ROM character generator. The character generator contains dot patterns for 256 characters. The character set contains the following major grouping of characters. Sixteen special characters for game support, 15 characters for support of word processing editing functions, the standard 96 ASCII graphic set, 48 characters to support foreign languages, 48 characters for business block graphics allowing drawing of charts, boxes and tables using single and double lines, 16 of the most often used Greek characters, and 15 of the most often used scientific notation characters.

The Color/Graphics Monitor Adapter function is packaged on a single card which fits into one of the five System Expansions Slots on the System Board. The direct drive and composite video ports are rightangle mounted connectors at the rear of the adapter and extend through the rear panel of the System Unit.

The display adapter is implemented using a Motorola 6845 CRT controller device. This adapter is highly programmable with respect to raster and character parameters. Thus, many additional modes are possible with clever programming of the adapter. A block diagram of the Color/Graphics Adapter is on the following page.



Figure 15. COLOR/GRAPHICS MONITOR ADAPTER BLOCK DIAGRAM

A.M.

Color/Graphics Monitor Adapter Block Diagram

Major Components Definitions

Motorola 6845 CRT Controller

This device provides the necessary interface to drive a raster scan CRT.

Mode Set And Status Registers

This is a general purpose programmable I/O register. It has I/O points which may be individually programmed. Its function in this attachment is to provide mode selection (page 2-49 and 2-50) and color selection in the medium resolution color graphics mode (page 2-51.)

Display Buffer

The Display Buffer resides in the CPU address space starting at address X'B8000'. It provides 16K bytes of dynamic read/write memory. A dual-ported implementation allows the CPU and the graphics control unit to access this buffer. The CPU and the CRT control unit have equal access to this buffer during all modes of operation except in high resolution alphanumeric mode. In this mode the CPU should access this buffer during the horizontal retrace intervals. The CPU may however, write to the required buffer at any time, but a small amount of display fetches will result if not during retrace intervals.

Character Generator

This attachment utilizes a ROM character generator. It consists of 8K bytes of storage which cannot be read/written under software control. This is a general purpose ROM character generator with three different character fonts. Two character fonts are used on this card (a 7x7 double dot and 5x7 single dot), selected by a card jumper. No jumper gives a 7x7 double dot, with a jumper a single dot font is selected.

Timing Generator

This block generates the timing signals used by the 6845 CRT controller and by the dynamic memory. It also resolves the CPU/ graphic controller contentions for accessing the Display Buffer.

Composite Color Generator

The logic in this block generates base band video color information.

Modes of Operation

There are two basic modes of operation, 'Alphanumeric' and 'Graphics'. Each of these modes provide further options in both color and black-and-white. The following text describes each mode of operation.

Alphanumeric Mode

Alphanumeric Display Architecture

Every display character position is defined by two bytes in the regen buffer (part of display adapter, not system memory). Both the color and the black and white display adapter use this 2 byte character/attribute format.

DISP	LAY	CHAR	CODE	BYTE				ATTRIBUTE BYTE								
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	

Attribute Byte Definition

ATTRIBUTE FUNCTION

ATTRIBUTE BYTE

7	6	5	4	3	2	1	0
В	R	G	В	1	R	G	В
FG	BAC	KGRO	UND	FOR	REGRO	UND	
В	0	0	0	1	1	1	1
В	٦	1	1	1	0	0	0
В	0	0	0	1	0	0	0
В	1	1	1	1	1	1	1

I = HIGH LIGHT FOREGROUND (CHAR) B= BLINK FOREGROUND (CHAR)

Color TV

NORMAL

REVERSE VIDEO NON DISPLAY (BLK) NON DISPLAY (WHITE)

- Display up to 25 rows of 40 characters each
- Maximum of 256 characters
- Requires 2000 bytes of Read/Write Memory (on the adapter)
- 8x8 character box
- 7x7 double dotted characters (one descender)
- Character attributes (one for each character)



Note: The starting address of the display buffer must be an even location.

Color Monitor (with Direct Drive input capability)

Display up to 25 rows of 80 characters each

Requires 4000 bytes of Read/Write Memory (on the adapter)

Maximum of 256 character set

8x8 character box

7x7 character with one descender

Same format for attributes as for color TV

Note: The starting address of the display buffer must be an even location.

IBM Monochrome Display Adapter Vs. Color/ Graphics Adapter Attribute Relationship

Table 3. Monochrome Vs Color/Graphics Attributes



Note: Not all Monitors Recognize the (1) Bit

(I) BIT

Table 4. Color/Graphics Modes

	HORIZONTAL	VERTICAL	NO OF COLORS (INCL. BACKGROUND COLOR)
LOW RES	160	100	16 (INCLUDES BLACK AND WHITE)
MED RES	320	200	4 COLORS: 1 OF 16 FOR BACKGROUND PLUS GREEN, RED, YELLOW OR CYAN, MAGENTA, WHITE
HIGH RES	640	200	B & W ONLY

- 1.
- Low resolution color graphics (TV or monitor). (<u>Note:</u> This mode is not supported in ROM).
 - Up to 100 rows of 160 pels each (2x2)
 - 1 of 16 colors each pel specified by I, R, G and B
 - Requires 8000 byte of Read/Write Memory (on the adapter)
 - Memory mapped graphics (requires special memory map and set up to be defined later)
- 2. Medium resolution color graphics (TV or monitor)
 - Up to 200 rows of 320 pels each (1x1)
 - 1 out of 4 preselected colors in each box
 - Requires 16000 bytes of Read/Write Memory (on the adapter)
 - Memory mapped graphics

4 pels/byte



• Graphics storage is organized in two banks of 8000 bytes each.

Graphics Storage Map

Memory Address



Address #0000 contains pel information for upper left corner of display area.

Color selection is determined by the following logic:

C1 and C0 will select 4 of 16 preselected colors.

This color selection (palette) is preloaded in an I/O port.

- C1 C0 CODE SELECT COLOR FOR DISPLAY POSITION
- 0 0 DOT TAKES ON COLOR OF 1 OF 16 PRESELECTED BACKGROUND COLORS.
- 0 1 SELECT 1ST COLOR OF PRESELECT COLOR SET "1" OR "2"
 - 0 SELECT 2ND COLOR OF PRESELECT COLOR SET "1" OR "2"
- 1 1 SELECT 3RD COLOR OF PRESELECT COLOR SET "1" OR "2"

The two color sets are:

1

SET ONESET TVCOLOR 1 - CYANCOLOFCOLOR 2 - MAGENTACOLOFCOLOR 3 - WHITECOLOF

<u>SET TWO</u> COLOR 1 - GREEN COLOR 2 - RED COLOR 3- BROWN

The background colors are the same basic 8 color as defined for low resolution graphic plus 8 alternate intensities defined by the intensity bit for a total of 16 color including black and white.

- 3. Black and white high resolution graphics (monitor)
 - Up to 200 rows of 640 pels each (1x1)
 - Black and white only
 - Requires 16000 bytes of Read/Write Memory (on the adapter)
 - Addressing and mapping is the same as for medium resolution color graphics, but the data format is different. In this mode each bit in memory is mapped to a pel on the screen.
 - 8 pels/byte



Description of Basic Operations

In the alphanumeric mode the adapter fetches character and attribute information from its display buffer. The starting address of the display buffer is programmable through the 6845, but it must be an even address. The character codes and attributes are then displayed according to their relative position in the buffer.



The CPU and the display control unit have equal access to the display buffer during all the operating modes except high resolution alphanumeric. During this mode, the CPU should access the display buffer during the vertical retrace time (if not, then the display will be affected with random patterns as the CPU is using the display buffer). The characters are displayed from a prestored "character generator" which contains the dot patterns of all the displayable characters.

In the graphics mode the displayed dots and colors are also fetched from the display buffer (up to 16K bytes). In the Color/Graphics Mode Section, the bit configuration for each graphics mode is explained.

Table 5. Summary of Available Colors

	I	R	G	В	COLOR
	0	0	0	0	Black
	0	0	0	1	Blue
	0	0	1	0	Green
-	0	0	1	1	Cyan
	0	1	0	0	Red
	0	1	0	1	Magenta
	0	1	1	0	Brown
	0	1	1	1	Light Gray
	1	0	0	0	Dark Gray
	1	0	0	1	Light Blue
	1	0	1	0	Light Green
	1	0	1	1	Light Cyan
	1	1	0	0	Light Red
	1	1	0	1	Light Magenta
	1	1	1	0	Yellow
	1	1	1	1	White
			_		

Note: "I" provides extra luminance (brightness) to each shade available. Resulting in the light colors listed above, except where the "I" bit is not recognized by some monitors.

Programming Considerations

Programming the 6845 CRT Controller

The 6845 has 19 internal registers which are used to define and control a raster scanned CRT display. One of these registers, the Address Register, is actually used as a pointer to the other 18 registers. It is a write only register which is loaded from the CPU by executing an OUT instruction to I/O address 3D4. The five least significant bits of the I/O bus are loaded into the Address Register.

In order to load any of the other 18 registers, the Address Register is first loaded with the necessary pointer and then the CPU may output a value to I/O address 3D5 in order to load the information in the preselected register.

The following table defines the values which must be loaded in 6845 Registers in order to control the different modes of operation supported by the attachment.

Programming the Mode Control and Status Register

The following I/O devices are defined on the Color/Graphics Adapter.

HEX ADDR.	A9	A8	A7	A6	A5	A4	A3	A2	A1	AO	FUNCTION OF REGISTER
X'3D8'	1	1	1	1	0	1	1	0	0	0	DO REG (MODE CONTROL)
X,3D8,	1	1	1	1	0	1	1	0	0	1	DO REG (COLOR SELECT)
X'3DA'	1	1	1	1	0	1	1	0	1	0	DI REG (STATUS)
X'3DB'	1	1	1	1	0	1	1	0	1	1	CLEAR LIGHT PEN LATCH
X'3DC'	1	1	1	1	0	1	1	1	0	0	PRE SET LIGHT PEN LATCH
X'3D0'	1	1	1	1	0	1	0	Ζ	Ζ	0	6845 REGISTERS
X'3D1'	1	1	1	1	0	1	0	Ζ	Ζ	1	6845 REGISTERS
X'3D0'	1	1	1	1	0	1	0	Z	Ζ	0	6845 REGISTERS
X'3D1'	1	1	1	1	0	1	0	Ζ	Ζ	1	6845 REGISTERS

Z = don't care condition

Color Select Register

This is a 6 bit output only, register, it can not be read, its address is X'3D9' and can be written using the 8088 I/O OUT command.

The following is a description of the Register functions.

the second se	
Bit O	B (BLUE) Border Color Select ALPHA/BACKGROUND
Bit 1	G (GREEN) Border Color Select ALPHA/BACKGROUND
Bit 2	R (RED) Border Color Select ALPHA/BACKGROUND
Bit 3	I Intensifies Border Color Select ALPHA/BACKGROUND IN 320 x 200
Bit 4	Select Alt Back Color Set For Alpha Color Modes
Bit 5	320 x 200 Color Set Select
Bit 6	Not Used
Bit 7	Not Used

Bits 0, 1, 2, 3. Select the screens border color in 40x25 alpha mode. In graphics mode (medium resolution) 320×200 color, the screen background color (C0-C1) is selected by these bit settings.

Bit 4. This bit when set will select on alternate, intensified, set of background colors in the alpha mode.

Bit 5 is only used in the medium resolution color mode (320×200). It is used to select the active set of screen colors for the display.

When bit 5 is set to a "1" colors are determined as follows.

- The C1 C0 Set selected are:
 - 0 0 Background as defined by Bit 0-3 of Port '3D9'
 - 0 1 Cyan
 - 1 0 Magenta 1
 - White 1

When bit 5 is set to a "0" Colors are determined as follows.

- The C0 C1 Set selected are:
 - 0 0 Background as defined by Bit 0-3 of Port '3D9'
 - 0 1 Green 1
 - 0 Red
 - 1 Yellow 0

Mode Select Register

This is a 6 bit output only register, it can not be read. Its address is X'3D8'. It can be written using the 8088 I/O OUT command.

The following is a description of the registers functions.

Bit 0

- Bit 0 80 x 25 mode
- Bit 1 Graphic Select
- Bit 2 B & W Select
- Bit 3 Enable Video Signal
- Bit 4 High Res 640 x 200 B & W Mode
- Bit 5 Change BACKGROUND INTENSITY to Blink Bit
- Bit 6 Not Used
- Bit 7 Not Used
- Bit 0 Selects between 40 x 25 and 80 x 25 alpha mode, a "1" sets it to 80 x 25 mode.
- Bit 1 Selects between ALPHA mode and 320 x 200 graphics mode, a "1" select 320 x 200 graphics mode.
- Bit 2 Selects color or B & W mode, a "1" selects B & W.
- Bit 3 Enables the video signal at certain times when modes are being changed. The video signal should be disabled when changing modes. A "1" enables the video signal.
- Bit 4 When on, this bit selects the 640 x 200 B & W graphics mode. One color of 8 can be selected on direct drive sets in this mode by using register 3D9.
- 2-62

When on, this bit will change the character background intensity to the blinking attribute function for ALPHA modes. When the high order attribute bit is not selected, 16 background colors (or intensified colors) are available. For normal operation, this bit should be set to "1" to allow the blinking function.

Mode Register Summary

Bits

Bit 5



z = don't care condition

* THE LOW RESOLUTION 160 x 100 MODE REQUIRES SPECIAL PROGRAMMING AND IS SET UP AS ALPHA MODE 40 x 25

Status Register

The status register is a 4 bit read only register. Its address is X'3DA'. It can be read using the 8088 I/O IN instruction.

The following is a description of the register functions.

- Bit 0 Display Enable
- Bit 1 Light Pen Trigger Set
- Bit 2 Light Pen SW Made
- Bit 3 Alpha Dots
- Bit 4 Not Used
- Bit 5 Not Used
- Bit 6 Not Used
- Bit 7 Not Used
- Bit 0 This input bit, when active, indicates that a regen buffer memory access can be made without interfering with the Display.
- Bit 1 This bit, when active, indicates that a positive going edge from the light pen input has set the light pen trigger. This trigger is reset on power on and may also be cleared by doing an I/O OUT command to address X'3DB'. No specific data setting is required, the action is address activated.
- Bit 2 The light pen switch status is reflected in this status bit. The switch is not latched or debounced. A "0" indicates the switch is on.
- Bit 3 The ALPHA video output signal is readable in this status bit. Its purpose is to verify that video information is being generated for RAS purposes.

Sequence of Events

- 1. Determine mode of operation
- 2. Reset Video Enable bit
- 3. Program 6845 to select mode
- 4. Program mode/color select registers

Memory Requirements

The memory used by this adapter is self-contained. It consists of 16k bytes of memory without parity. This memory is used as both a display buffer for alphanumeric data and as a bit map for graphics data. The Regen Buffers address starts at X'B8000'.

Interrupt Level (Vertical Retrace)

Level 2

I/O Address and Bit Map

Read/Write Memory Address Space



System Read/Write Memory

Display Buffer (16K Bytes)

128K RESERVED REGEN AREA

Display Buffer (16K Bytes)

EN AREA



Color/Graphics Monitor Adapter Direct Drive, and Composite Interface Pin Assignment





Color/Graphics Monitor Adapter Auxiliary Video Connectors



0

	_		
	+12 Volts	1	
RF Modulator	(key) Not Used	2	Color/Graphics
mountor	Composite Video Output	3	Audpter
	Logic Ground	4	
	RF Modulator Interface		
	– Light Pen Input	1	
	(key) Not Used	2	
Light	— Light Pen Switch	3	Color/Graphics
Pen	Chassis Ground	4	Adapter ent
	+ 5 Volts	5	
	+ 12 Volts	6	
	Light Pen Interface		L